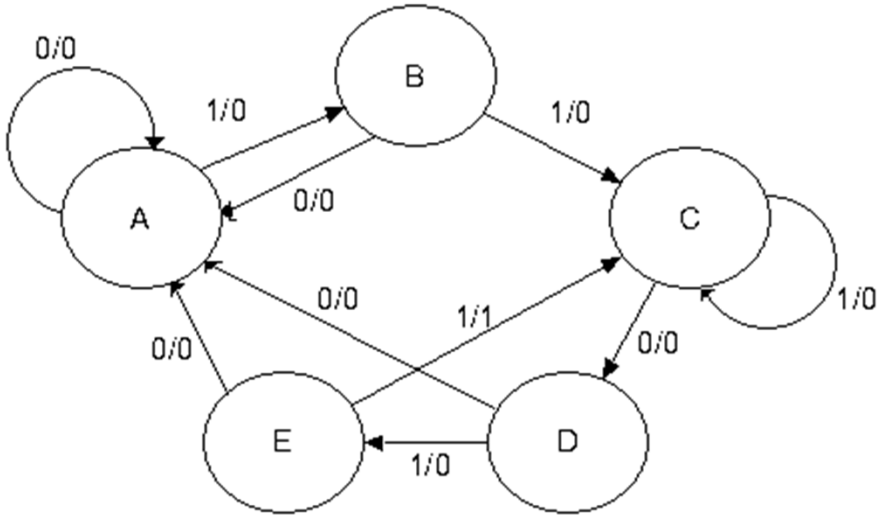
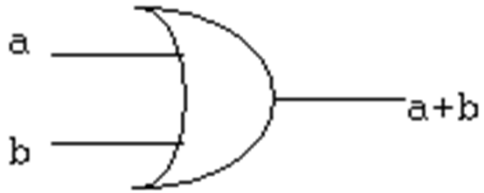
From a Bubble to the next…
That's how its done

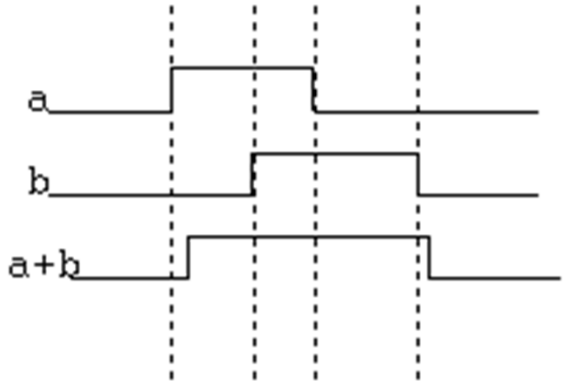
CSCI 255



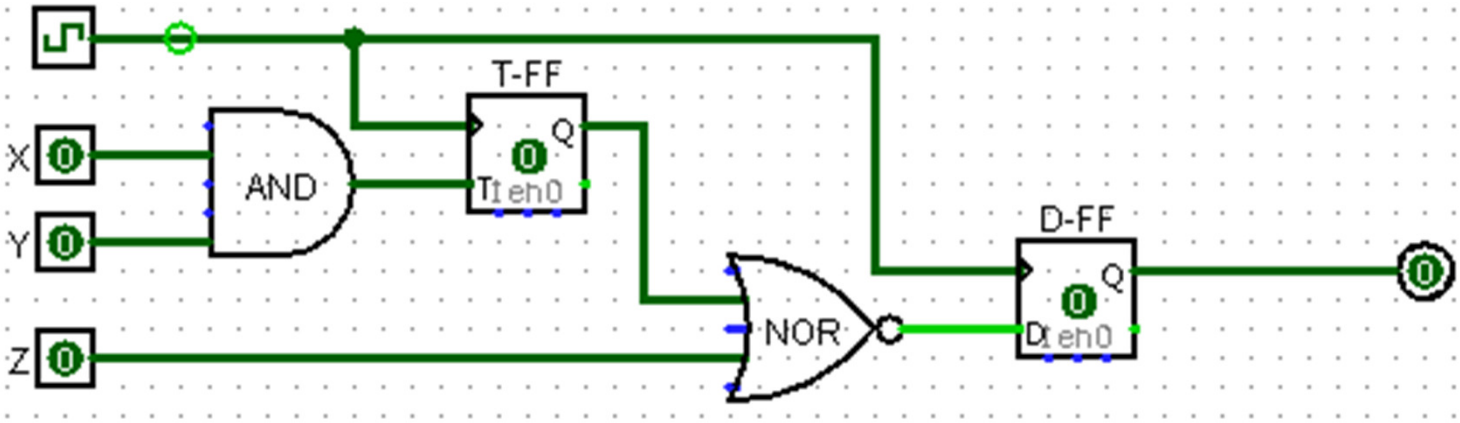
http://www.edwardbosworth.com/My5155Textbook_HTM/MyText5155_Ch07_V06.htm

- In class, latches and flip-flops were covered
- Time is the essential part of “remembering” values
- Examples are solved on these slides

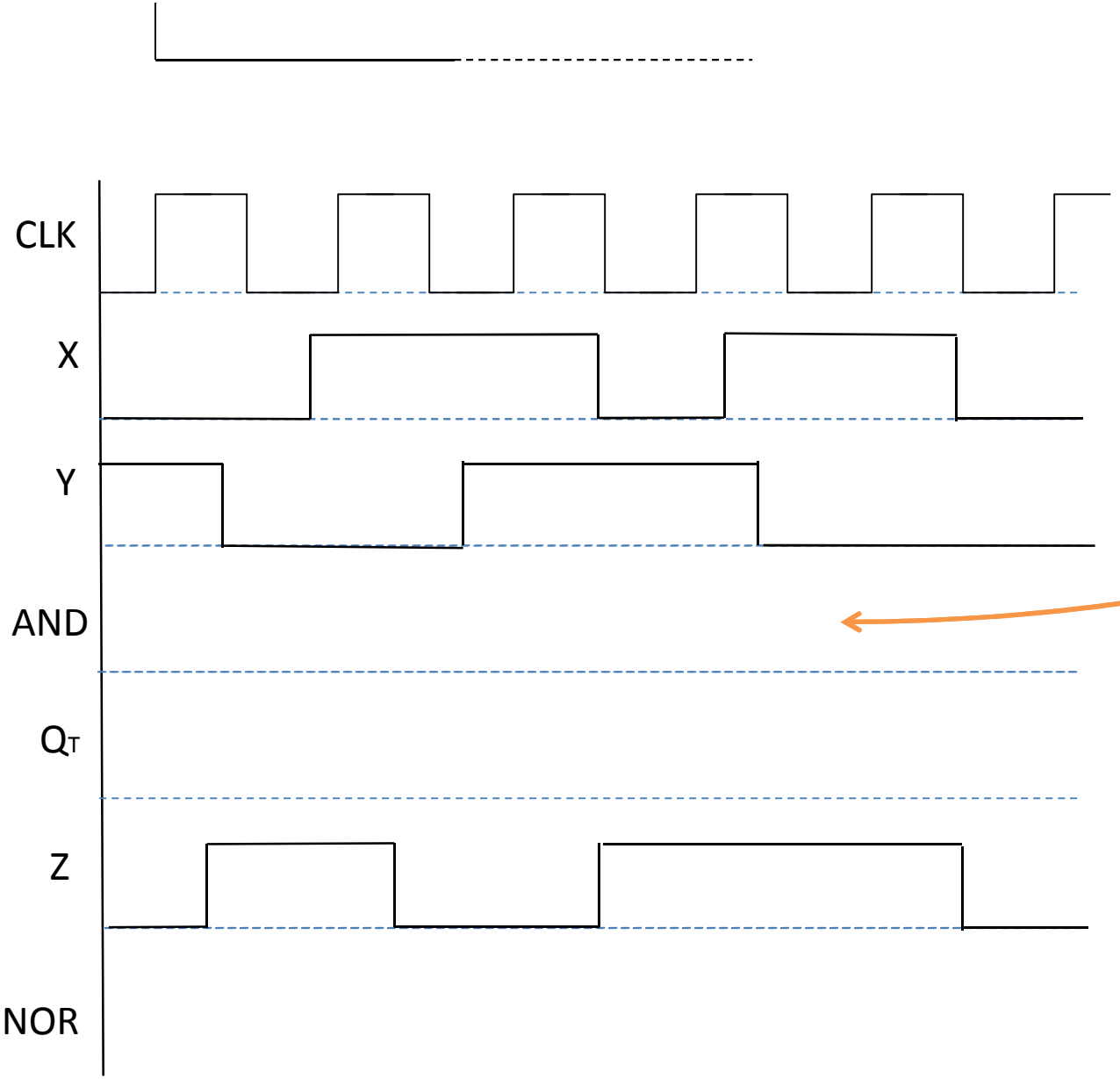




- Assume we need to time-evaluate the following circuit
- Circuit has a sequential & combinational components
- Assume all Qs = 0 @ time=0
- Assume FFs are Positive-Edge triggered

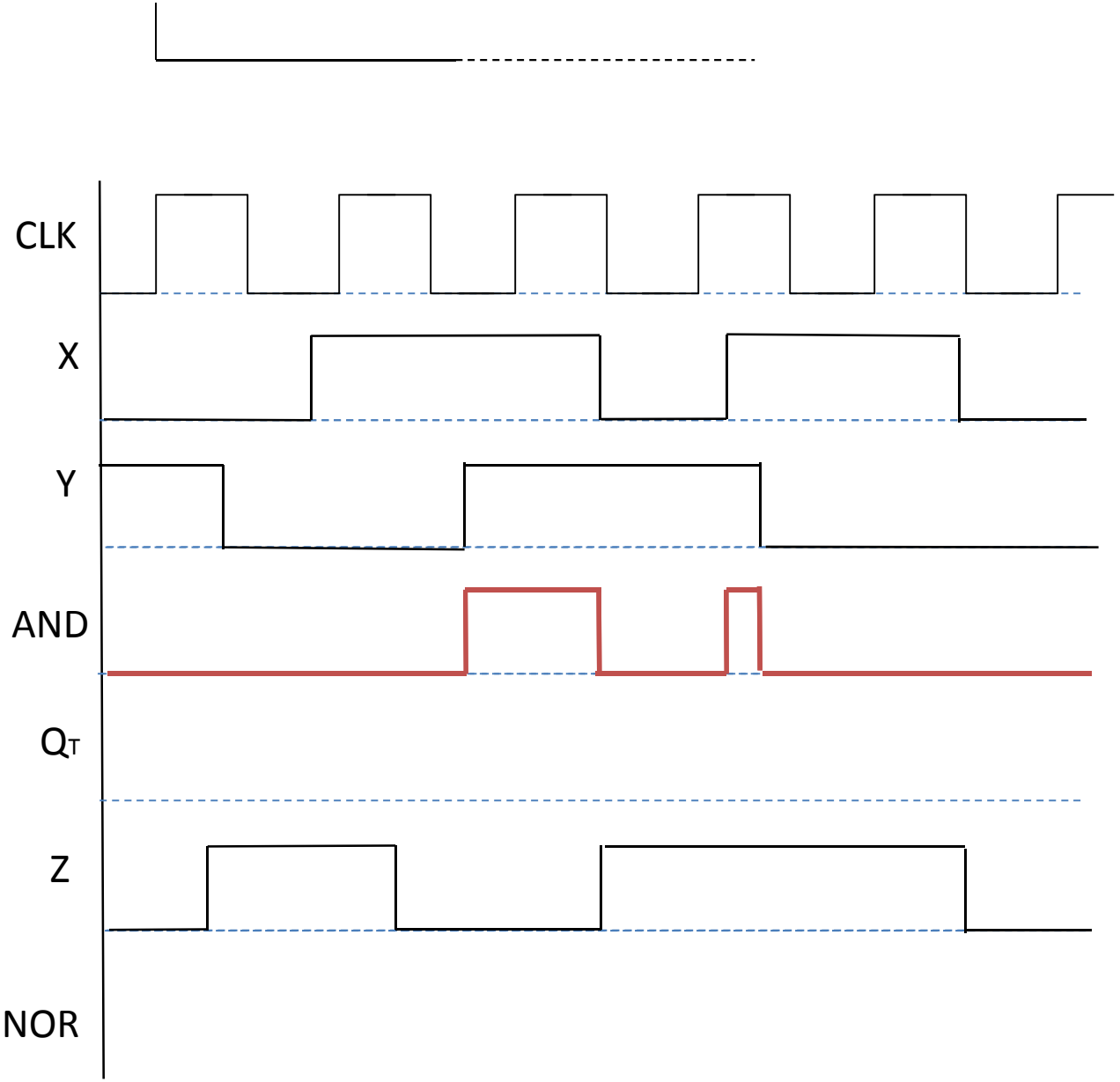


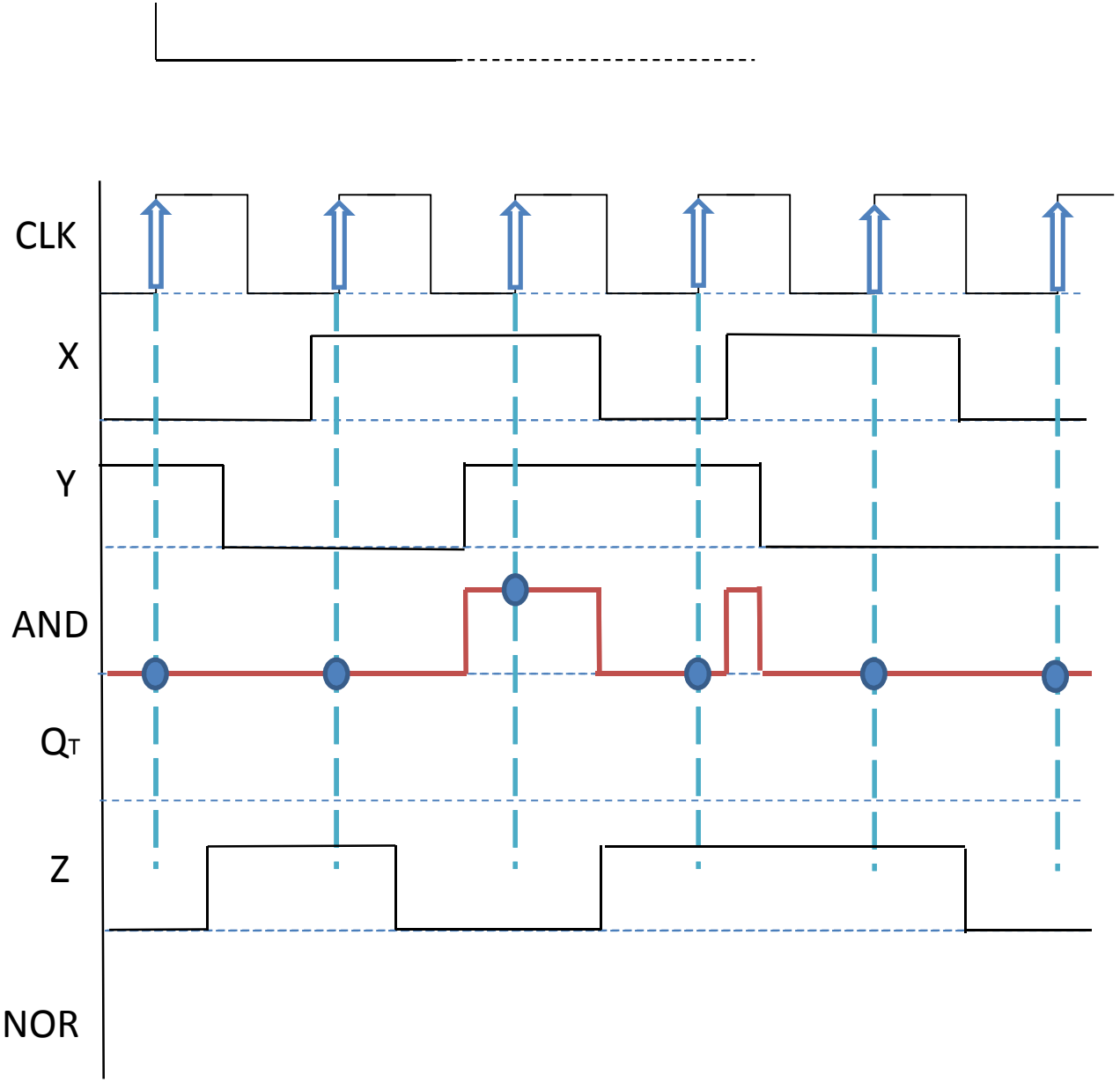
Sequential Circuits



We first want to analyze the inputs of the AND gate in order to know what are the values for the T-FF. The AND gate does not depend on TIME!

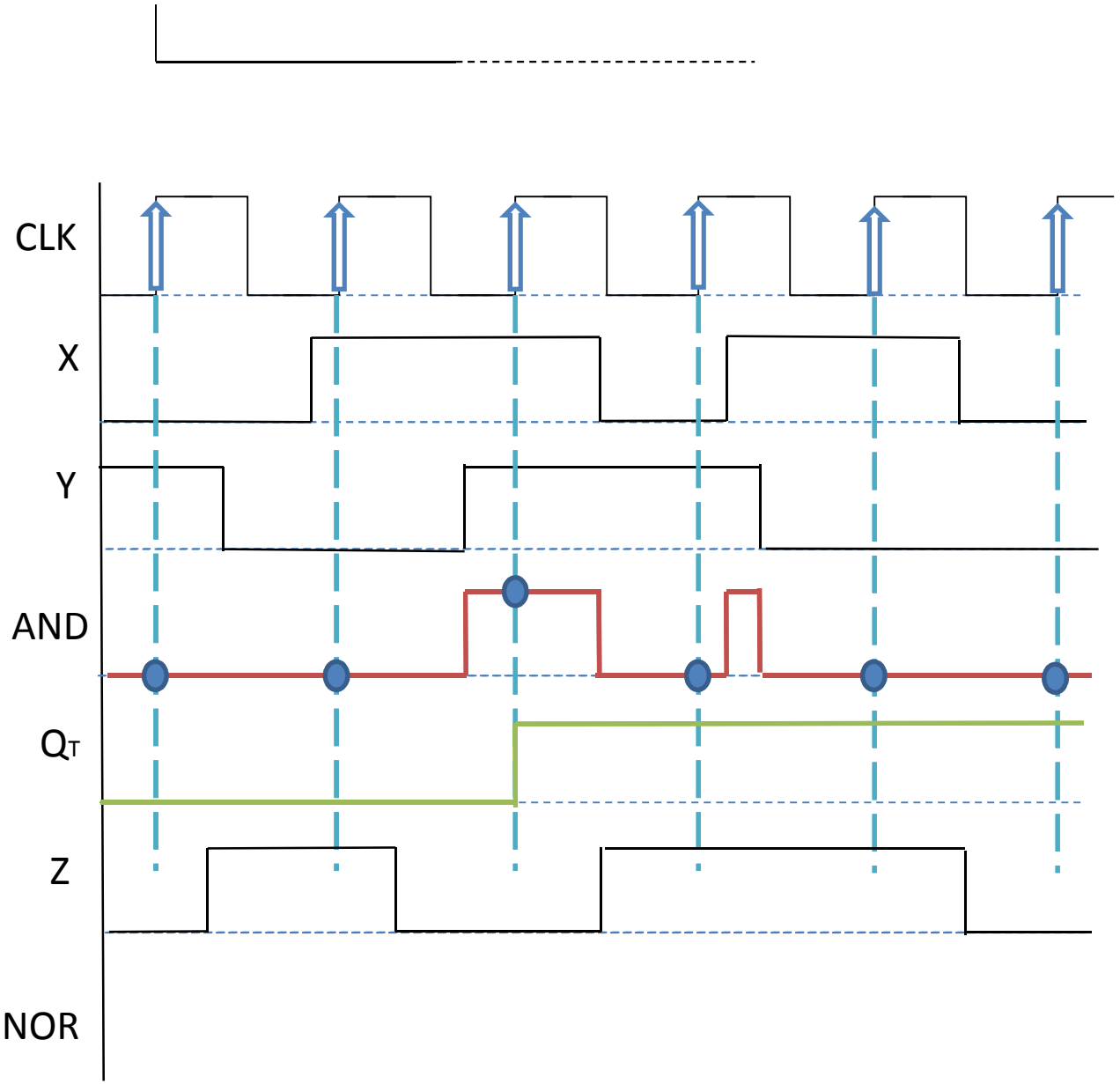
Sequential Circuits





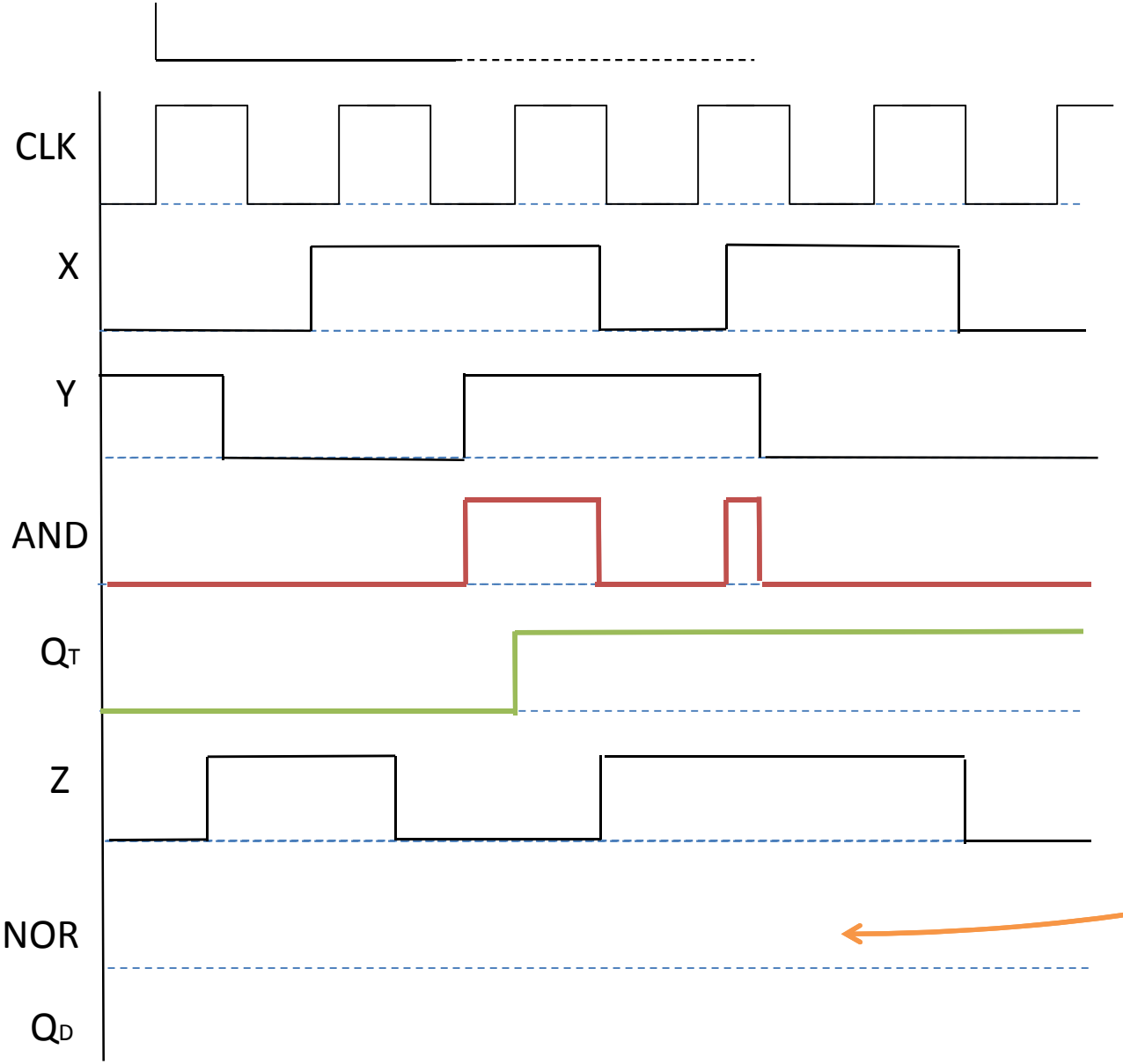
The timing result of the AND gate becomes the input signal of the T-Flip-Flop. Using the positive edge, we can then analyze Q_T. Q=0 @ t=0

Sequential Circuits



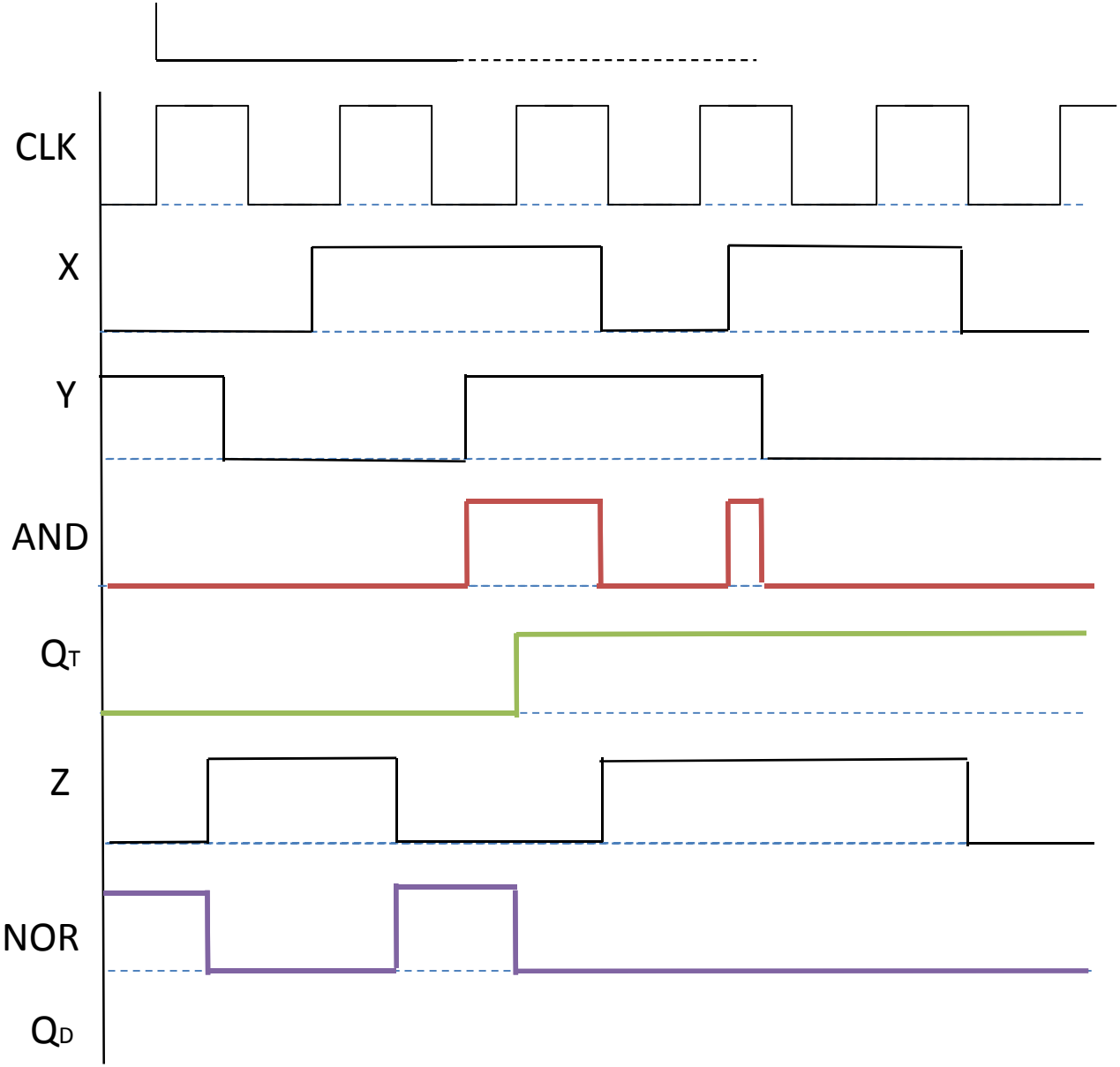
T	Q(t)	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Sequential Circuits

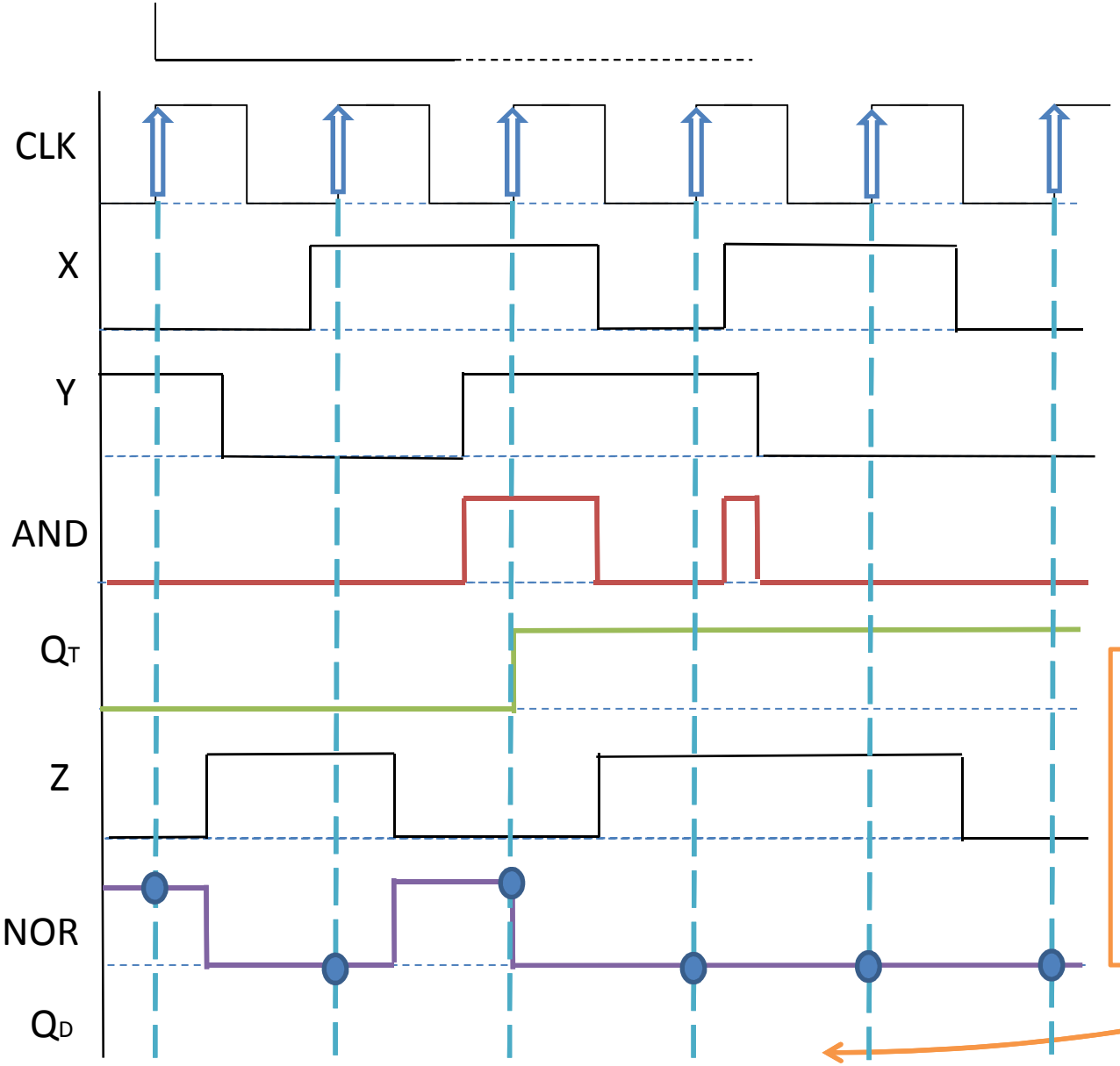


NOR Gate as the Z & Q_T inputs. NOR gate does not depend on the clock signal

Sequential Circuits

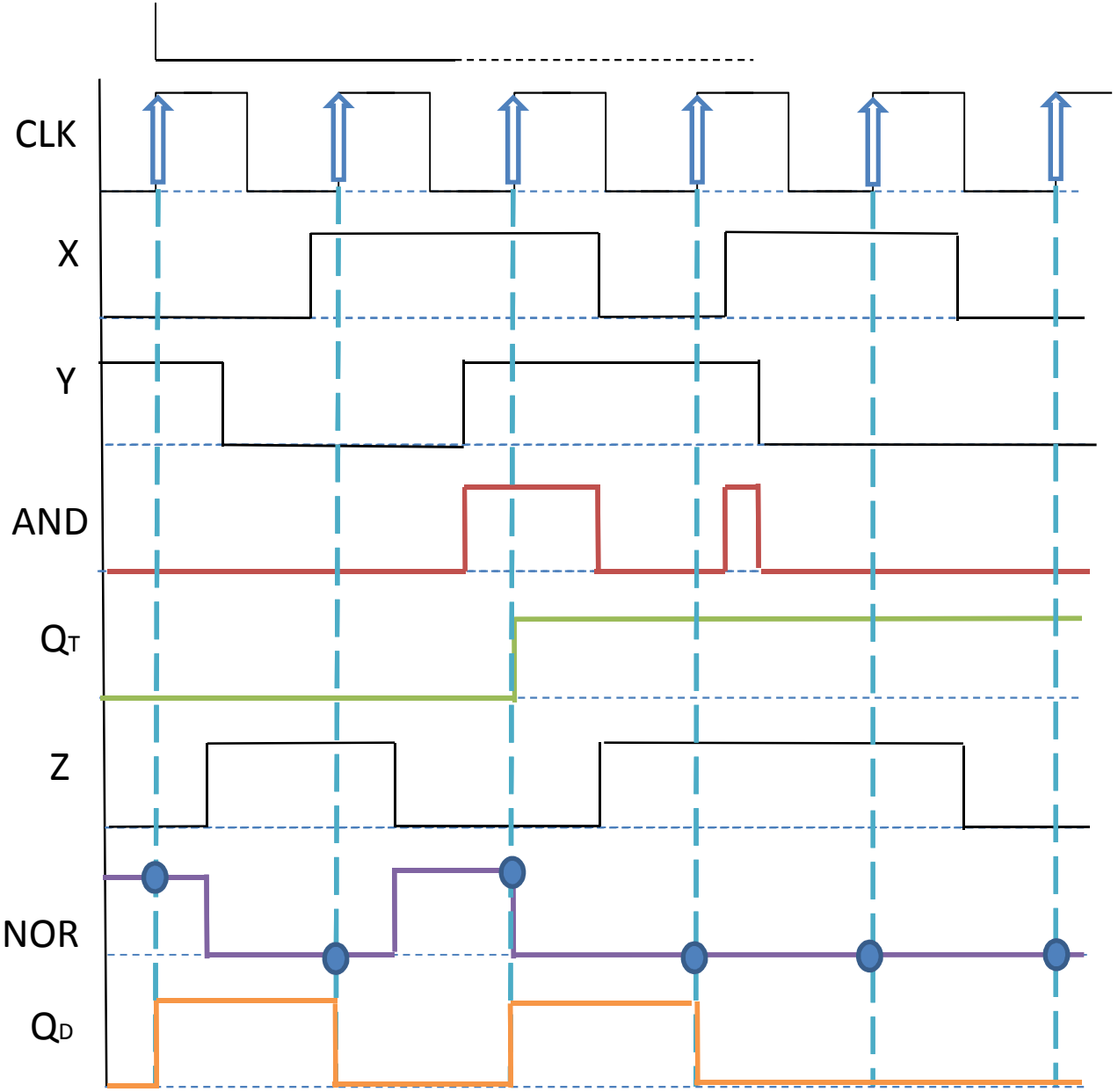


Sequential Circuits

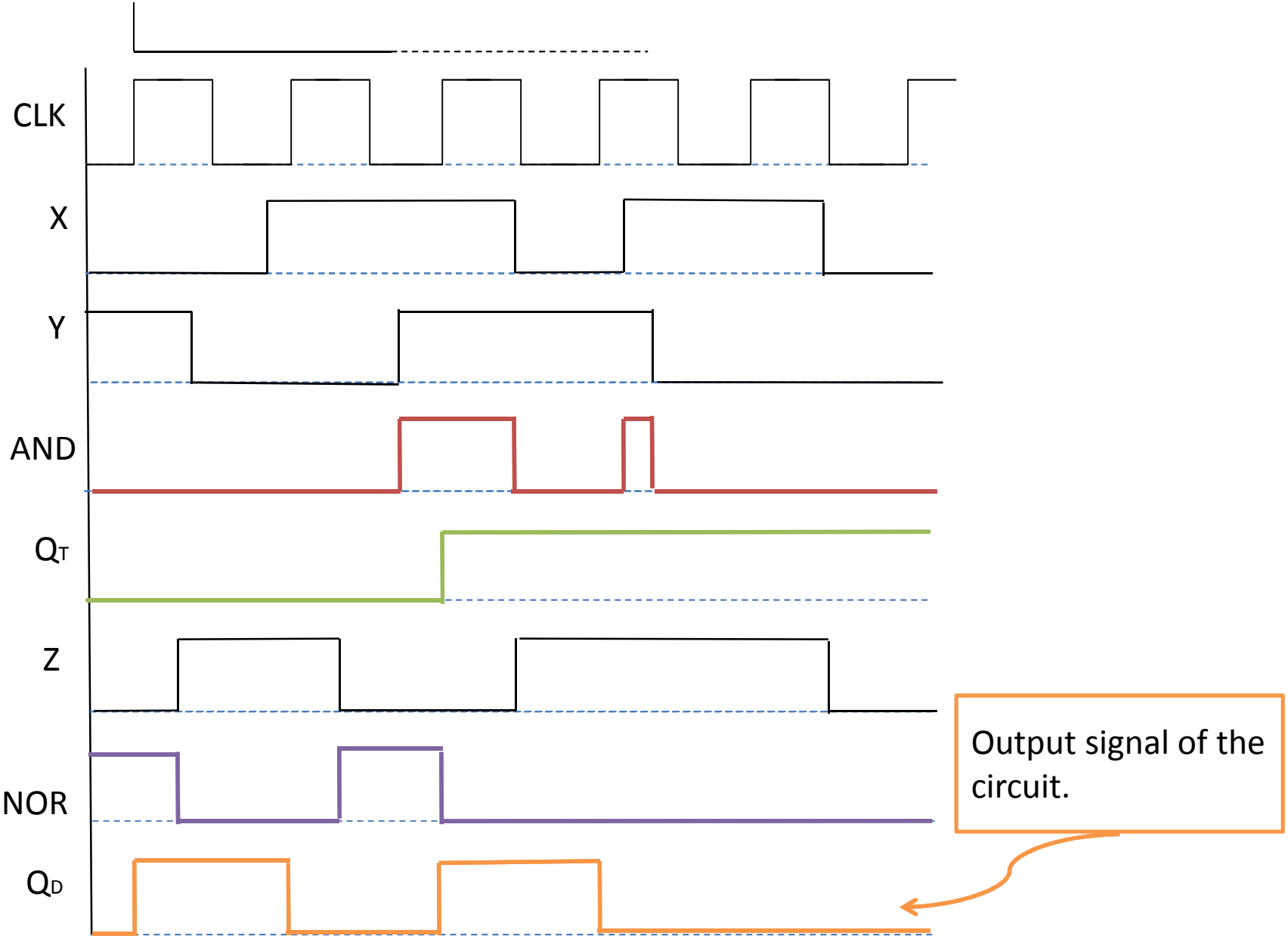


Q_D is obtained from what it reads from the D-input; which is the NOR signal in this case

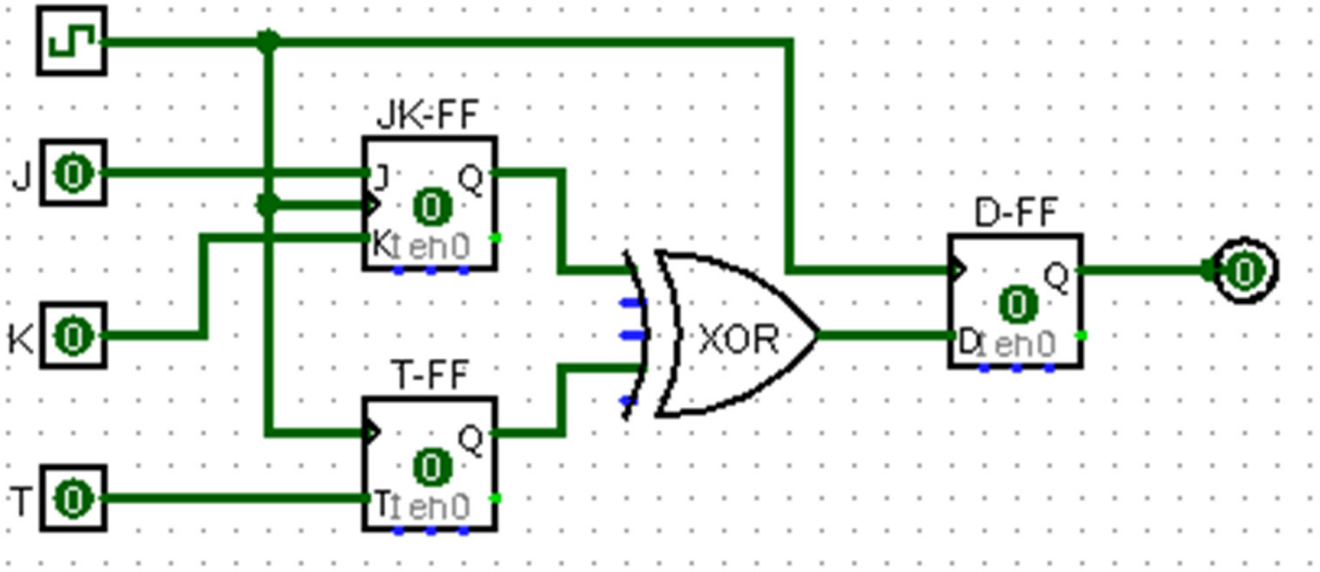
Sequential Circuits

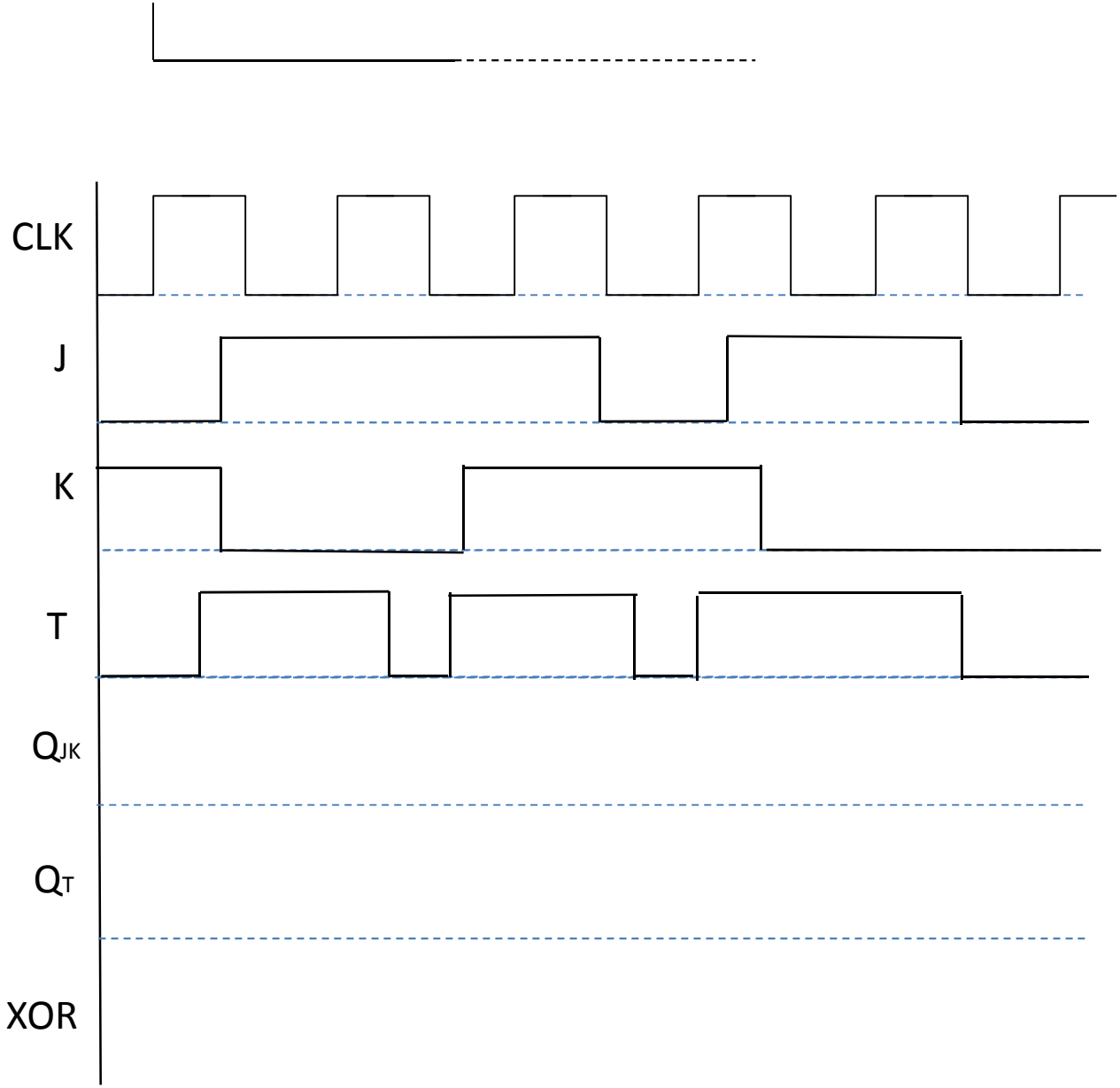


Sequential Circuits



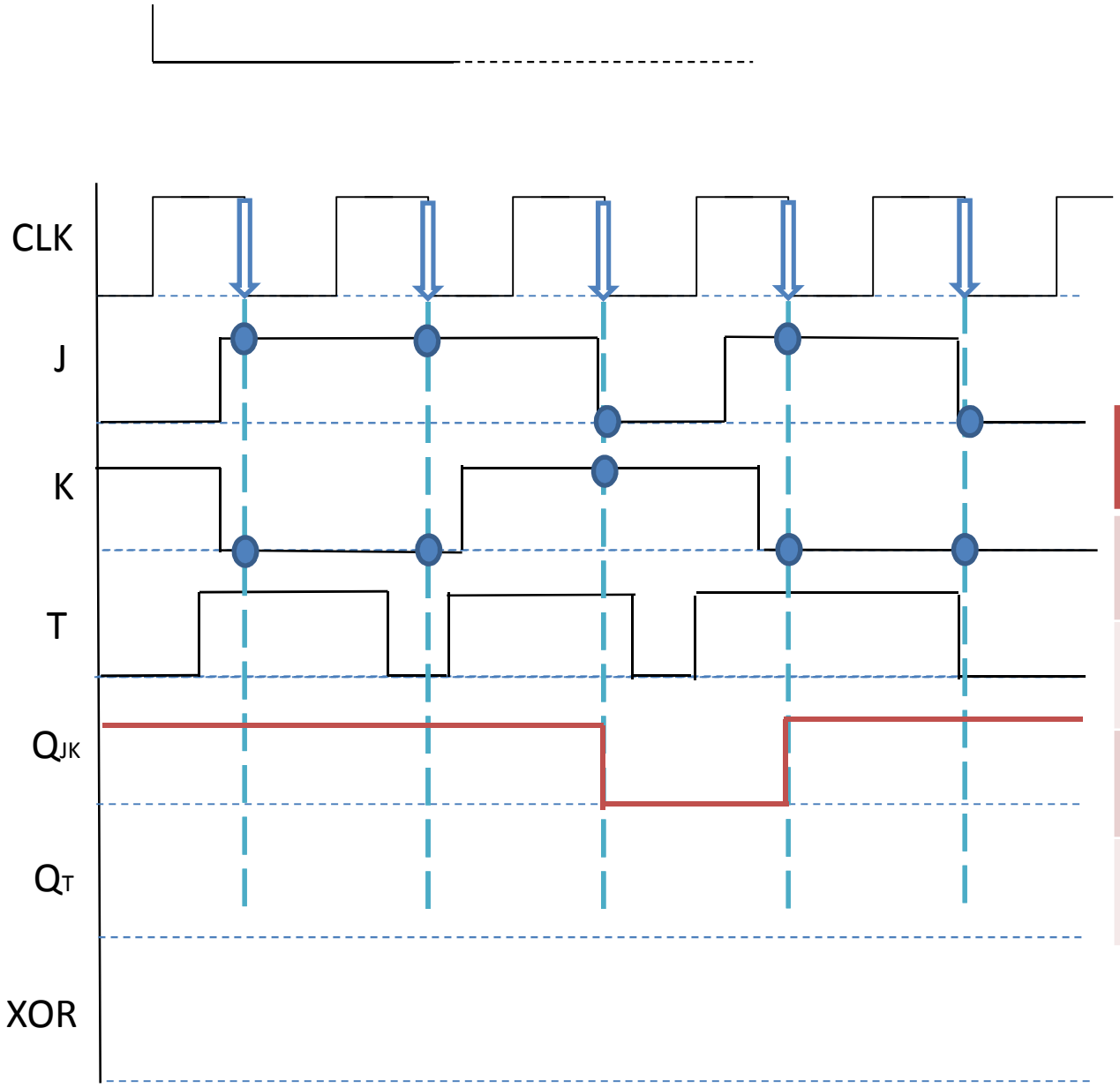
- Assume we need to time-evaluate the following circuit
- Circuit has a sequential & combinational components
- Assume all Qs = 1 @ time=0
- Assume FFs are Negative-Edge triggered





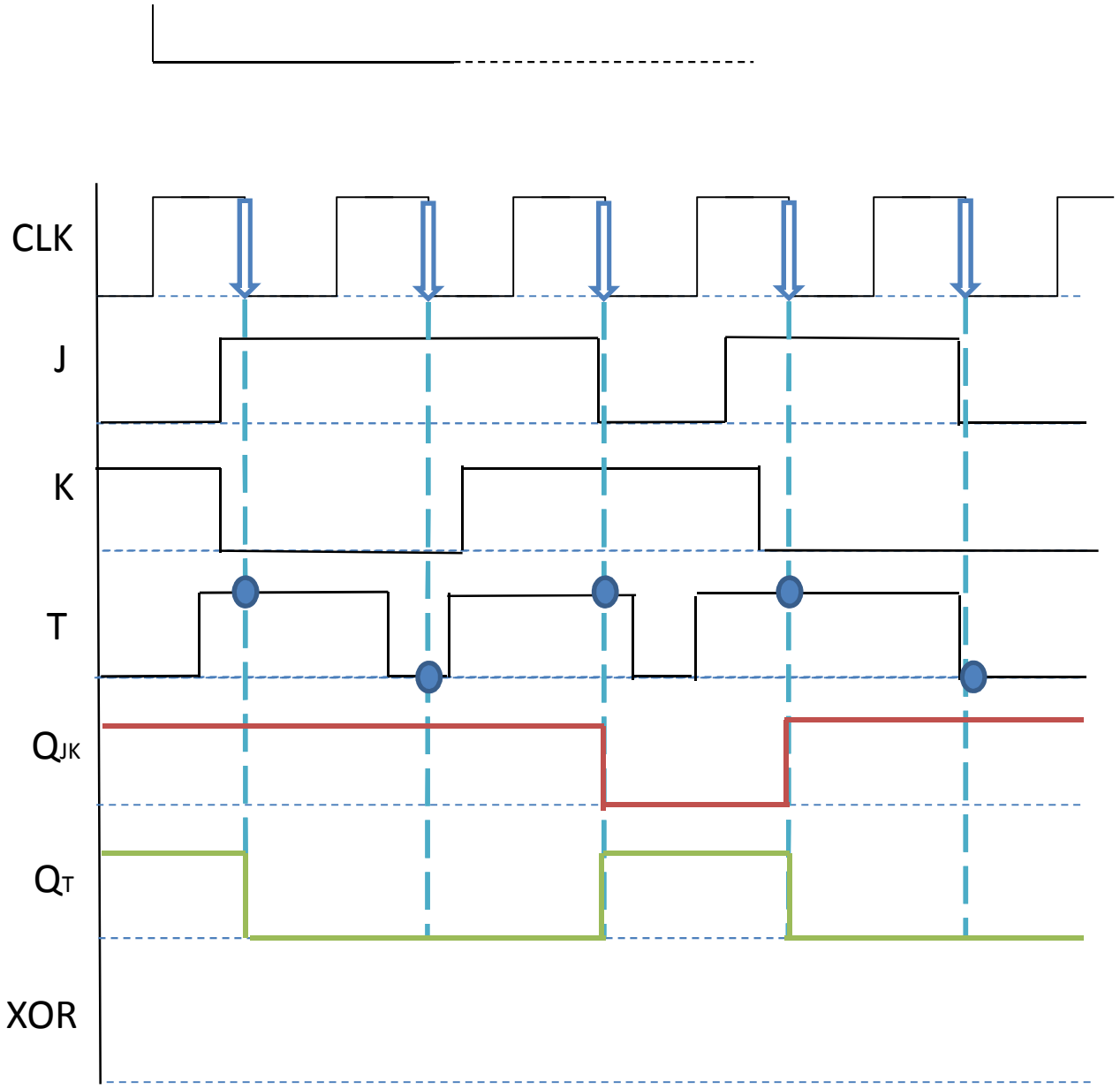
In this case, you can perform the JK & T flip flop diagrams at the same time, but to avoid mistakes…. We'll draw up JK first

Sequential Circuits



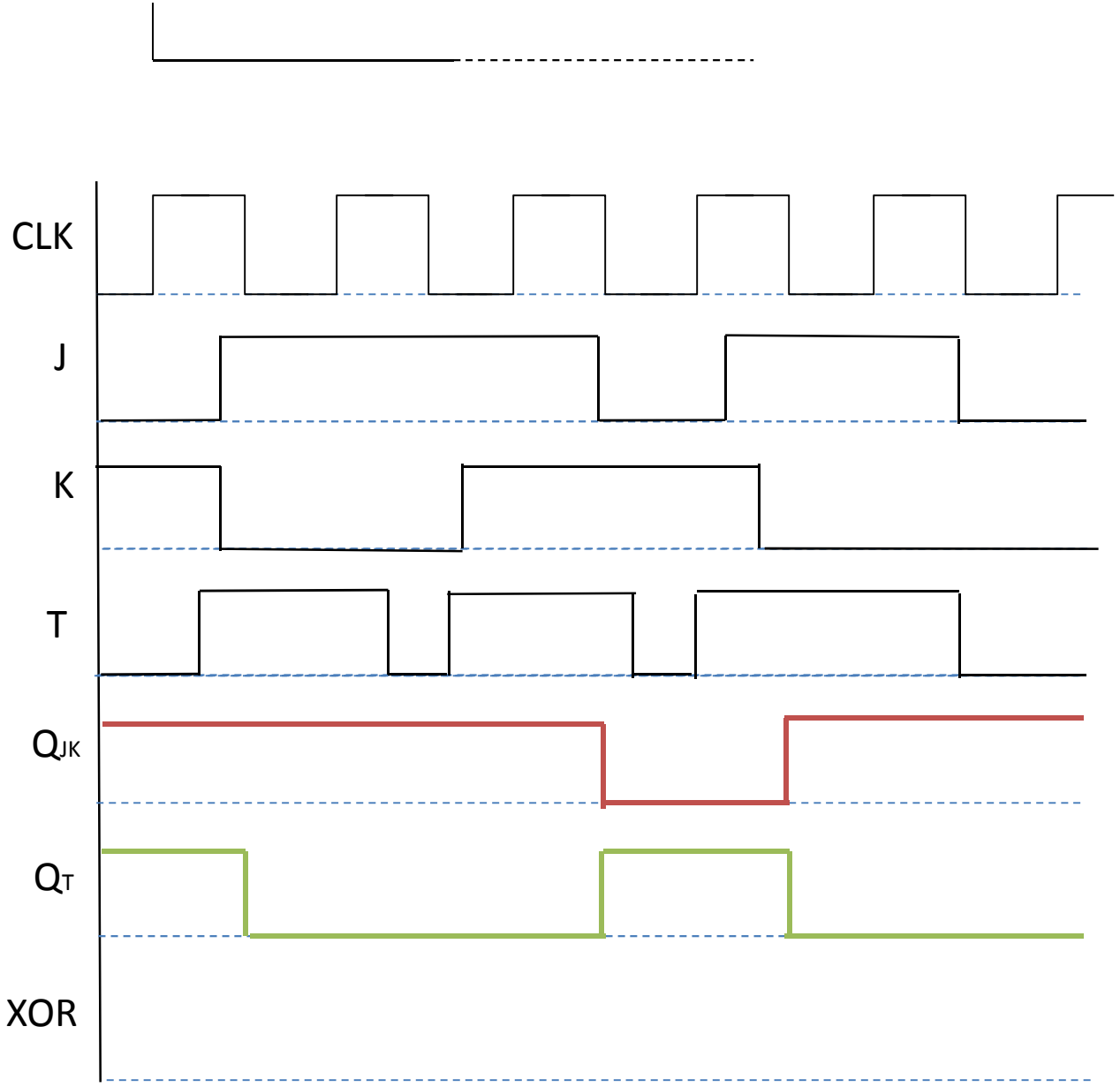
J	K	Q(t)	Q (t+1)
0	X	0	0
1	X	0	1
X	1	1	0
X	0	1	1

Sequential Circuits



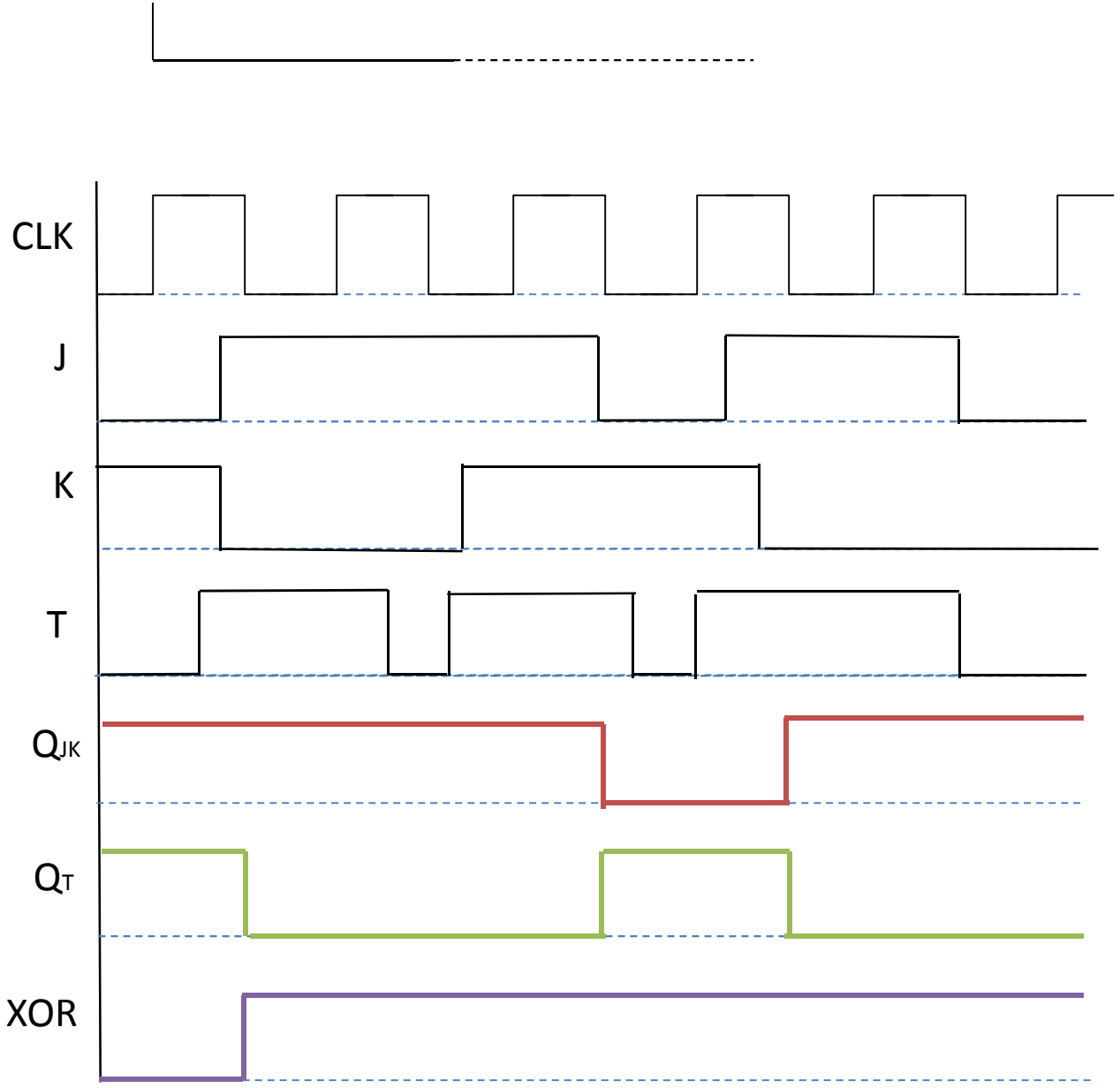
T	Q(t)	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Sequential Circuits

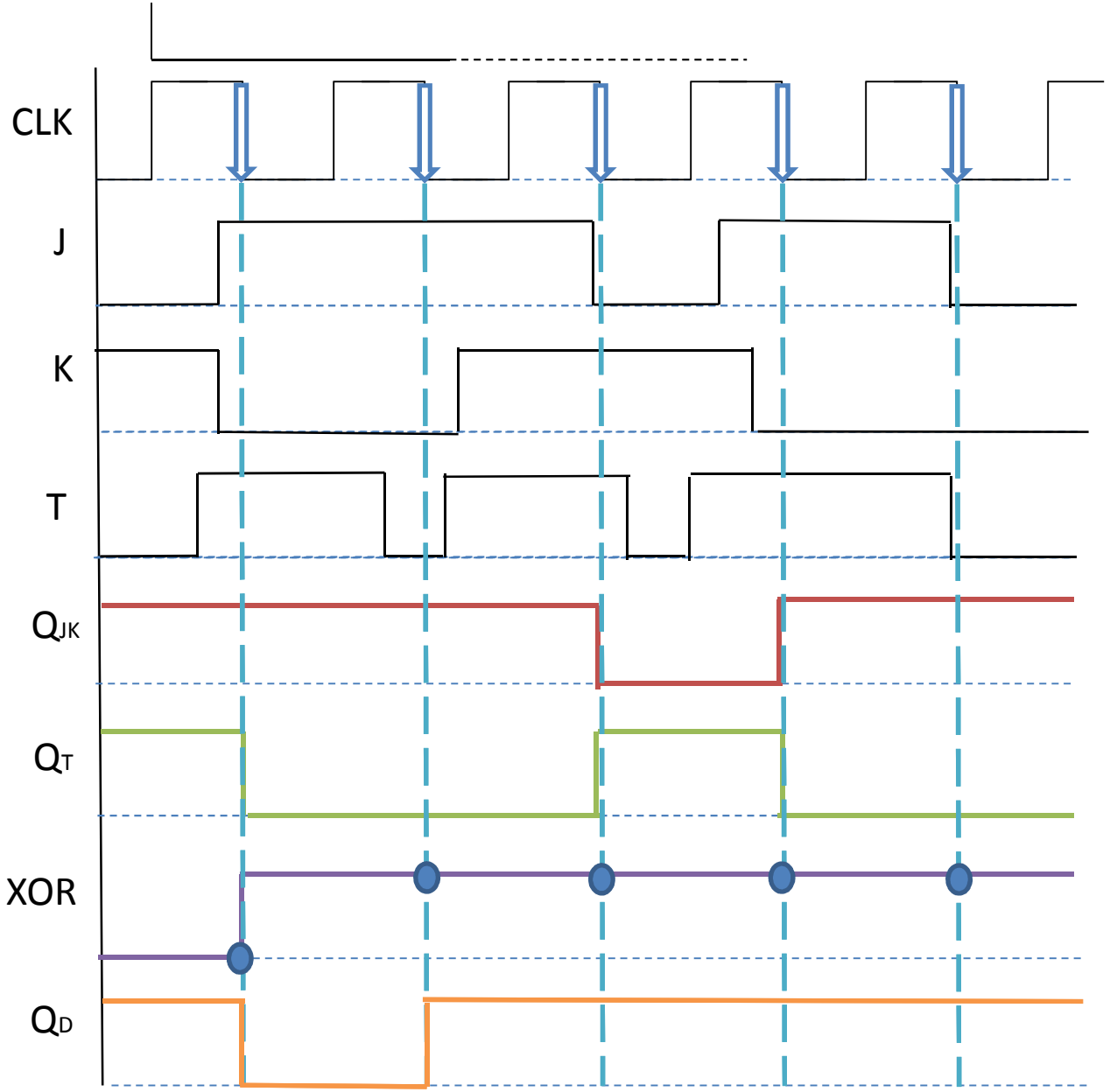


XOR the JK & T resulting signals. XOR does not depend on the clock signal

Sequential Circuits

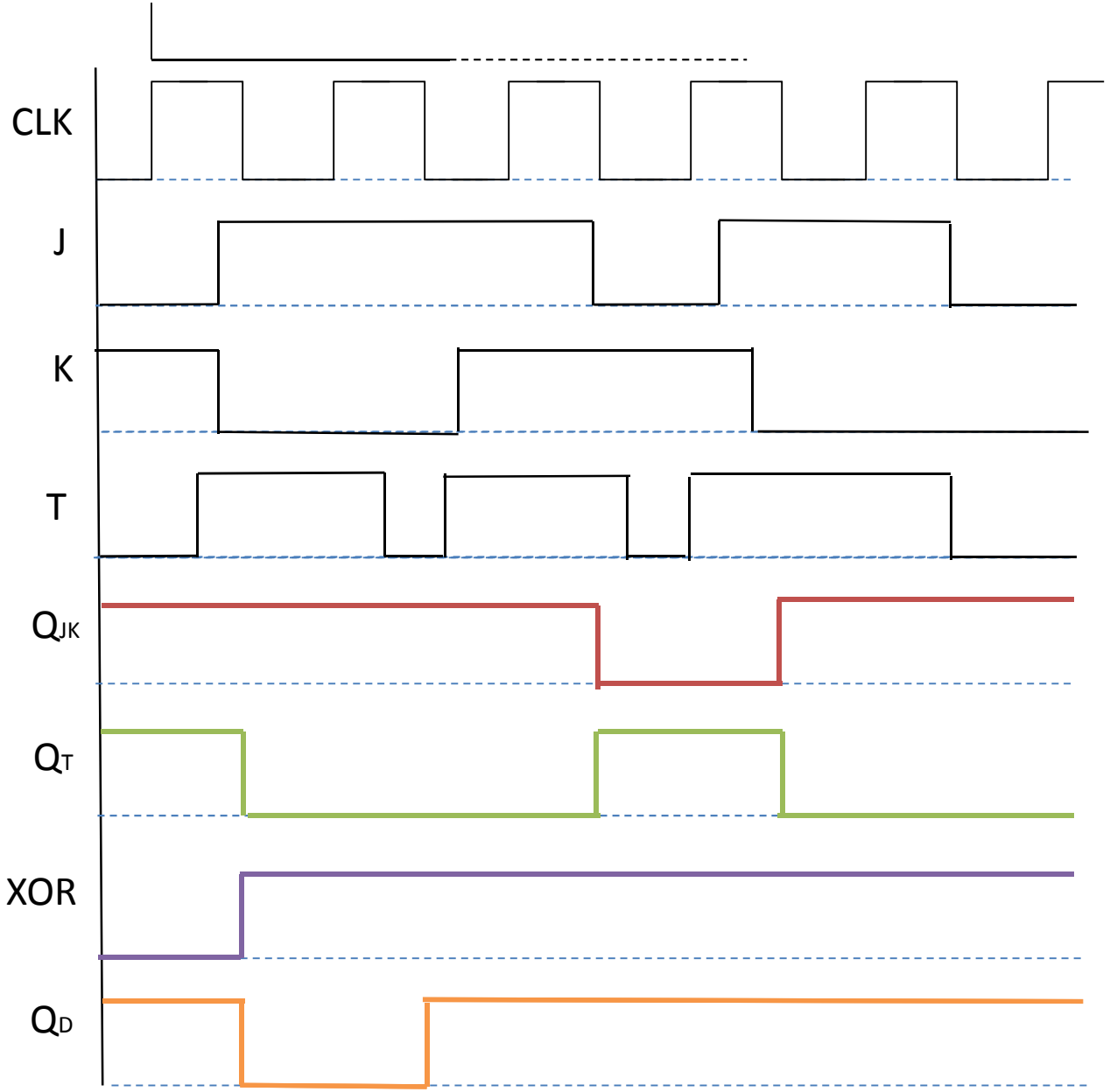


Sequential Circuits



D-FF input signal is the XOR resultant signal.

Sequential Circuits



Output signal of the circuit